JEDEC STANDARD

Short Circuit Withstand Time Test Method

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JEDEC SOLID STATE TECHNOLOGY ASSOCIATION

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SHORT CIRCUIT WITHSTAND TIME TEST METHOD

(From Council Ballot JCB-91-52 formulated under the cognizance of JC-25 Committee on Transistors)

1. PURPOSE

In some circuits, such as motor drives, it is necessary for a semiconductor device to withstand a short circuit condition for short periods of time. During such a condition, the current in the device is dependent on the gain of the device and the level of the drive supplied. It is important for the designer to know how long a device can survive a short circuit condition with a given drive level. Fault detect circuits can be designed to react within this time period.

In some case the junction temperature may exceed the maximum rating. If it does, the rating shall be nonrepetitive with a limit on the maximum number of events over the lifetime of the device. Otherwise, it will be a repetitive rating. In the case of a nonrepetitive rating, the manufacturer shall perform adequate reliability testing so as to ensure the validity of this rating. If the specification is a military one, then the controlling document shall mandate such tests.

2. SCOPE

All power semiconductors or hybrids that can be turned off with a control terminal and are designed to be used as a switching device. Power MOSFETs, IGBTs, and bipolar transistors are examples of these devices.

3. CIRCUITRY

As shown in Figure 1, electrical test circuity to test short circuit endurance is very simple. Drive circuitry must be appropriate for the device tested, whether voltage or current driven. Care must be taken to minimize stray inductance in the output circuit in order to avoid limiting the current during the test, or avalanching the device during turn off at the end of the test.

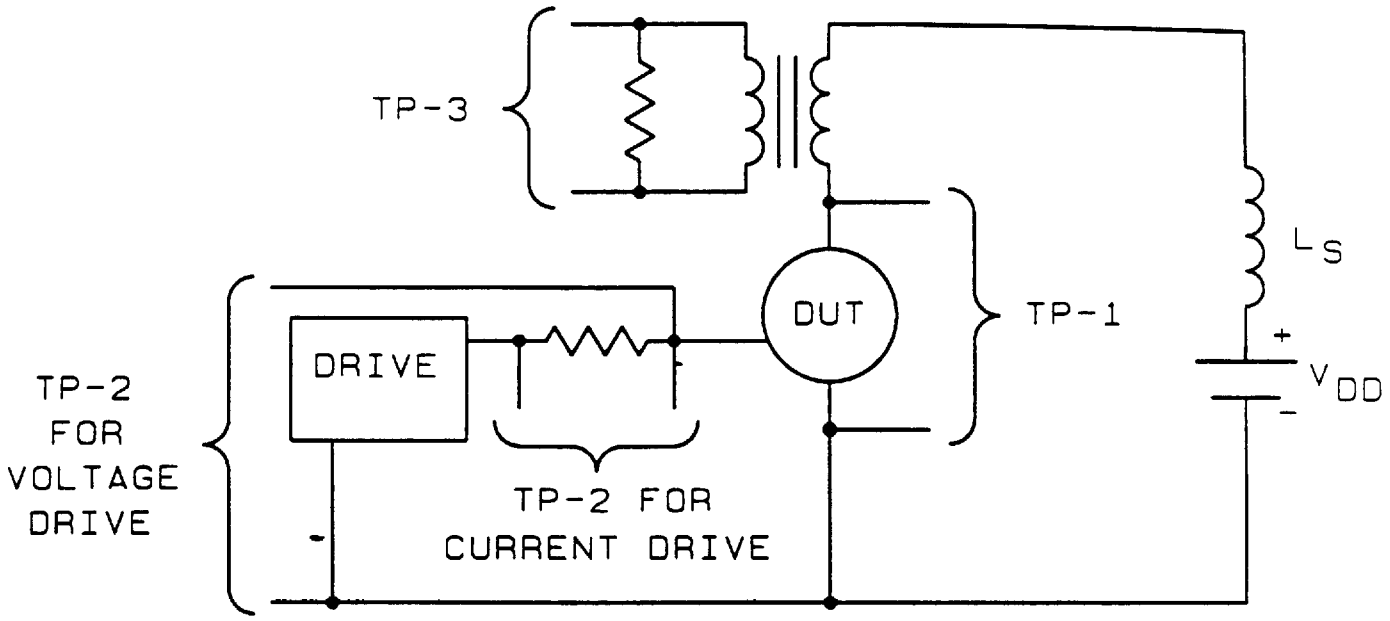

Figure 1
Electrical Test Circuitry

4. DEFINITIONS

T_j = Junction temperature (°C). Its starting value shall be specified, and controlled to 5% at the beginning of the test.

t_{sc} = Short circuit withstand time (seconds). Measured between the instant when the device drive rises to 50% of its peak value, and the instant when it falls to 50% of its peak value.

V_{sc} = Nominal short circuit voltage (volts). Must be maintained within +5% and -10% of the specified value during the test.

Drive = One of the following:

V_{DRIVE} = Nominal drive voltage (volts).

I_{DRIVE} = Nominal drive current (amperes).

This value must be maintained to within $\pm$5% of the specified value. In a graphical representation, various levels of "drive" may be specified, as shown in Figure 2. The speed of turn-off shall be such that avalanching the DUT is prevented.

L_S = Stray inductance of the output circuit shall be kept as low as is practicable. In order to limit the value of L_S, the maximum value shall be a condition of the test that is determined by the device specification. See Figure 3. L_S = V dt/di during the first 10% of the output current waveform.

R_{DRIVE} = The output impedance of the drive circuitry.

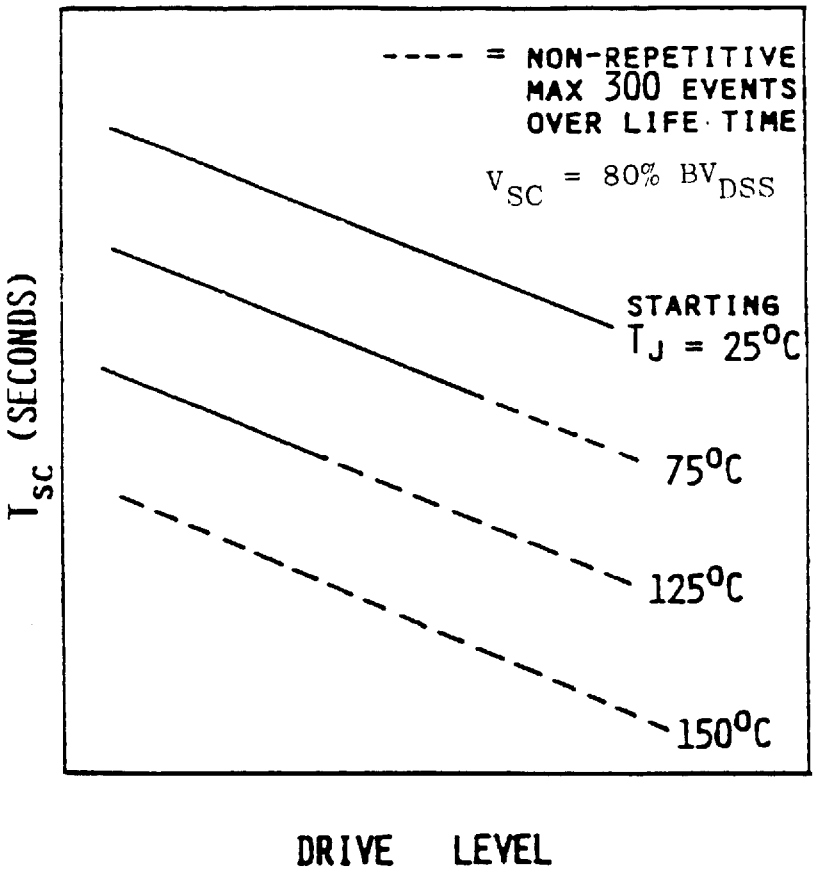

Figure 2
Sample Graphical Specification

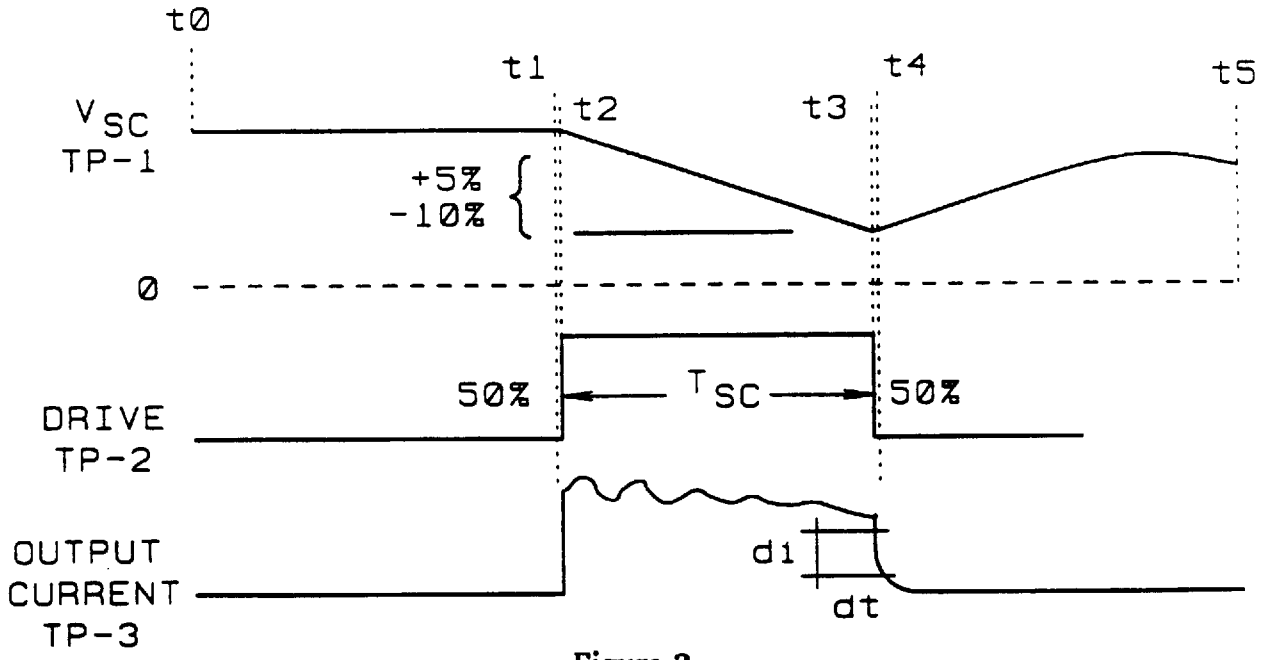

Figure 3

5. PROCEDURE

t0 - Apply test voltage.

t1 - Apply drive signal.

t2 - Device drive reaches 50% of maximum value.

t3 - Remove drive signal.

t4 - Device drive falls to 50% of maximum value.

t5 - Remove test voltage.

6. ACCEPTANCE CRITERIA

DC electrical test shall be conducted before and after the test. Exactly which parameters are to be measured will be device dependent, and shall be called out on the detailed specification.

7. SPECIFICATION

Tabular specification shall be as follows:

t_{sc} X.X (us) @

V_{sc} = XXX (volts)

Drive = XX (volts) or XX (amperes)

T_J = XX °C

R_{DRIVE} = XX (ohms)

L_S < xx (nH)


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